



Web Results 1 - 10 of about 118 for **CRC reciprocal modulo "cyclic redundancy check"**. (0.31 seconds)

[PPT] Lecture 26 - CRC, LFSR, Power

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... By raising to powers (**modulo** $p(x)$), all non ... **CRC-32**: $G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16}$... therefore an equivalent metric (**reciprocal**) is energy per operation (E ...

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[PDF] Microsoft PowerPoint - lec26.ppt

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... Reading - XILINX IEEE 802.3 **Cyclic Redundancy Check** (pages 1 ... **CRC** decoding ... a Galois (finite) field if we take the results of this multiplication **modulo** a prime ...

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[PDF] Optimal Rectangular Code for High Density Magnetic Tapes

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... increased, another check byte called **CRC (cyclic redundancy check)** was added ... practice ORC resembles the **CRC** single-track ... E denotes the summation **modulo** 2. The ...

www.research.ibm.com/journal/rd/186/ibmrd1806Q.pdf - [Similar pages](#)

[PDF] underlie error-control coding data computing, storage, and ...

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... $a(x)b(x) = c(x) \bmod (x^n + 1)$... For a cyclic code, the syndrome of an error $e(x)$ usually means the residue of $e(x) \bmod g(x)$, the generator polynomial. ...

www.research.ibm.com/journal/sj/081/ibmsj0801E.pdf - [Similar pages](#)

[PDF] Outline Channel Coding I Outline Channel Coding I

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Page 1. Volker Kühn Channel Coding I 1 Universität Bremen Outline Channel Coding I Outline Channel Coding I < Introduction @ Declarations ...

www.ant.uni-bremen.de/teaching/kc/kc1/slides/kc1_kap3.pdf - [Similar pages](#)

Universität Gesamthochschule Essen, Institut für experimentelle ...

... the error detection capabilities of an arbitrary **CRC**-Code. ... in the transmission, due to **reciprocal** disturbances of ... of solving the square roots **modulo** n , where ...

www.win.tue.nl/math/eidma/jaarverslagen/verslag94/node21.html - 17k - [Cached](#) - [Similar pages](#)

[PDF] Telemetry Channel Coding

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... Frames or Virtual Channel Data Units are used, references [1] and [2], respectively, require that a **cyclic redundancy check (CRC)** be used to ... **MODULO-2 ADDER**. ...

www.ccsds.org/CCSDS/documents/101x0b6.pdf - [Similar pages](#)

[PPT] Addl6302 Technology

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Page , Rev.2.6. 1997-2004, R.Levine. Information Coding for Transmission (Voice/Speech/Image Coding, error protection and encryption). ...

enr.smu.edu/~levine/ee8302/vcode4.ppt - [Similar pages](#)

[PDF] General Index

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... 698 in straight line fitting 663 CR method see Cyclic reduction (CR) Cramer'sV 631
Crank-Nicolson method 848, 853, 855 **CRC (cyclic redundancy check)** 896ff. ...
www.library.cornell.edu/nr/bookcpdf/c21-2.pdf - [Similar pages](#)

[PDF] **Fast of Software Implementation Error Detection Codes**

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... checksum, Fletcher checksum, CXOR checksum, **CRC** and WSC. ... s-complement integer arithmetic
modulo 2^s - 1 ... E. **Cyclic Redundancy Check Codes** **CRC** codes use modular ...
portal.acm.org/ft_gateway.cfm?id=219759&type=pdf - [Similar pages](#)

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Results Key:

JNL = Journal or Magazine **CNF** = Conference **STD** = Standard
1 **Fast incremental CRC updates for IP over ATM networks**
Braun, F.; Waldvogel, M.;

High Performance Switching and Routing, 2001 IEEE Workshop on , 29-31 Ma 2001

Pages:48 - 52

[\[Abstract\]](#) [\[PDF Full-Text \(96 KB\)\]](#) IEEE CNF
2 **VLSI layout generation of a programmable CRC chip**
Sait, S.M.; Tanvir, M.S.K.;

 Consumer Electronics, IEEE Transactions on , Volume: 39 , Issue: 4 , Nov 1995
Pages:911 - 916

[\[Abstract\]](#) [\[PDF Full-Text \(420 KB\)\]](#) IEEE JNL
3 **Hardware design and VLSI implementation of a byte-wise CRC gene chip**
Sait, S.M.; Hasan, W.;

 Consumer Electronics, IEEE Transactions on , Volume: 41 , Issue: 1 , Feb. 1993
Pages:195 - 200

[\[Abstract\]](#) [\[PDF Full-Text \(452 KB\)\]](#) IEEE JNL
4 **Error control aspects of high speed networks**
Dravida, S.;

INFOCOM '92. Eleventh Annual Joint Conference of the IEEE Computer and Communications Societies. IEEE , 4-8 May 1992

Pages:272 - 281 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(600 KB\)\]](#) IEEE CNF

5 Automatic generation of parallel CRC circuits*Sprachmann, M.;*

Design & Test of Computers, IEEE , Volume: 18 , Issue: 3 , May-June 2001

Pages:108 - 114

[\[Abstract\]](#) [\[PDF Full-Text \(92 KB\)\]](#) IEEE JNL

6 A symbol based algorithm for hardware implementation of cyclic redundancy check (CRC)*Nair, R.; Ryan, G.; Farzaneh, F.;*

VHDL International Users' Forum, 1997. Proceedings , 19-22 Oct. 1997

Pages:82 - 87

[\[Abstract\]](#) [\[PDF Full-Text \(380 KB\)\]](#) IEEE CNF

7 ATM framing using CRC byte*Dodds, D.E.; Lejin Du;*

Communications, 1994. ICC 94, SUPERCOMM/ICC '94, Conference Record, Se Humanity Through Communications. IEEE International Conference on , 1-5 M 1994

Pages:410 - 414 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(304 KB\)\]](#) IEEE CNF

8 Error-burst detection with tandem CRCs*Mazo, J.E.; Saltzberg, B.R.;*

Communications, IEEE Transactions on , Volume: 39 , Issue: 8 , Aug. 1991

Pages:1175 - 1178

[\[Abstract\]](#) [\[PDF Full-Text \(268 KB\)\]](#) IEEE JNL

9 A new parallel algorithm for CRC generation*Joshi, S.M.; Dubey, P.K.; Kaplan, M.A.;*

Communications, 2000. ICC 2000. 2000 IEEE International Conference on , Volume: 3 , 18-22 June 2000

Pages:1764 - 1768 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(436 KB\)\]](#) IEEE CNF

10 VLSI implementation of CRC-32 for 10 Gigabit Ethernet*Henriksson, T.; Eriksson, H.; Nordqvist, U.; Larsson-Edefors, P.; Liu, D.;*

Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE Internatio Conference on , Volume: 3 , 2-5 Sept. 2001

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[\[Abstract\]](#) [\[PDF Full-Text \(384 KB\)\]](#) IEEE CNF

11 Proposal of a timing model for CMOS logic gates driving a CRC /spl load*Hirata, A.; Onodera, H.; Tamaru, K.;*

Computer-Aided Design, 1998. ICCAD 98. Digest of Technical Papers. 1998

IEEE/ACM International Conference on , 8-12 Nov. 1998

Pages:537 - 544

[\[Abstract\]](#) [\[PDF Full-Text \(548 KB\)\]](#) IEEE CNF

12 A Comparison of Some Error Detecting CRC Code Standards

Witzke, K.; Leung, C.;

Communications, IEEE Transactions on [legacy, pre - 1988] , Volume: 33 ; Iss: 9 , Sep 1985

Pages:996 - 998

[\[Abstract\]](#) [\[PDF Full-Text \(296 KB\)\]](#) IEEE JNL

13 Variable rate data transmission with blind rate detection for coherent DS-CDMA mobile radio

Okumura, Y.; Adachi, F.;

Electronics Letters , Volume: 32 , Issue: 20 , 26 Sept. 1996

Pages:1865 - 1866

[\[Abstract\]](#) [\[PDF Full-Text \(264 KB\)\]](#) IEEE JNL

14 A self-timed cyclic redundancy check (CRC) in VLSI

Li, S.H.; Zukowski, C.A.;

Circuits and Systems, 1997. Proceedings of the 40th Midwest Symposium on , Volume: 2 , 3-6 Aug. 1997

Pages:1021 - 1025 vol.2

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15 A 4.25 GHz BiCMOS clock recovery circuit with an AV-DSPD architecture for NRZ data stream

Nakamura, S.; Tajima, A.; Kinoshita, Y.; Suemura, Y.; Fukaishi, M.; Suzuki, H.; Itani, T.; Miyamoto, H.; Henmi, N.; Yamazaki, T.; Yotsuyanagi, M.;

Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC 1997 IEEE International , 6-8 Feb. 1997

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[\[Abstract\]](#) [\[PDF Full-Text \(1060 KB\)\]](#) IEEE CNF

[1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [11](#) [12](#) [13](#) [14](#) [15](#) [16](#) [17](#) [18](#) [19](#) [Next](#)

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